

Appl. No. 09/560,673
Amdt. dated 01/19/2005
Reply to Office Action of 10/20/2004

REMARKS

This Amendment is in response to the Office Action mailed 10/20/2004. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Election/Restriction

2. The Examiner asserts that newly submitted claims 38-80 are directed to an invention that is independent or distinct from the invention originally claimed because the newly submitted claims include elements not included in the previously presented independent claims.

Applicant respectfully disagrees with the requirement for restriction and requests reconsideration and withdrawal or modification of the requirement. Applicant respectfully submits that the Examiner has misconstrued 37 CFR 1.145 which permits restriction of claims directed to an invention distinct from and independent of the invention previously claimed after an office action on an application.

§ 1.145 Subsequent presentation of claims for different invention.

If, after an office action on an application, the applicant presents claims directed to an invention distinct from and independent of the invention previously claimed, the applicant will be required to restrict the claims to the invention previously claimed if the amendment is entered, subject to reconsideration and review as provided in § 1.143 and § 1.144.

MPEP § 802.01 Meaning of "Independent" and "Distinct"

INDEPENDENT

The term "independent" (i.e., not dependent) means that there is no disclosed relationship between the two or more subjects disclosed, that is, they are unconnected in design, operation, or effect, for example: (1) species under a genus which species are not usable together as disclosed; or (2) process and apparatus incapable of being used in practicing the process.

DISTINCT

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The term "distinct" means that two or more subjects as disclosed are related, for example, as combination and part (subcombination) thereof, process and apparatus for its practice, process and product made, etc., but are capable of separate manufacture, use, or sale as claimed, AND ARE PATENTABLE (novel and unobvious) OVER EACH OTHER (though they may each be unpatentable because of the prior art). It will be noted that in this definition the term related is used as an alternative for dependent in referring to subjects other than independent subjects.

Newly submitted claims 38-80 were submitted in response to the Examiner's indication of allowable subject matter, now withdrawn. Each of the newly submitted independent claims includes all the elements of the base claims of a claim that was indicated as allowable. Therefore all the newly presented claims are "dependent" in the sense of having a disclosed relationship to the claims previously presented.

Newly presented claim 38 includes most of the elements of claim 12, the base claim and any intervening claims. The element of a shared buffer memory that appeared in intervening claim 11 has been omitted from claim 38. Applicant respectfully submits that the element of a shared buffer memory is not required for patentability of claim 38.

Newly presented claim 47 includes the elements of claim 32, the base claim and any intervening claims.

Newly presented claim 54 includes the elements of claim 36, the base claim and any intervening claims.

The newly presented claims are also not distinct because the two inventions indicated by the Examiner would not be patentable over each other. In particular, the base claims which are included in the newly presented claims would not be patentable over the newly presented claims.

Applicant respectfully requests that the Examiner withdraw the requirement for restriction and requests that newly presented claims 38-80 be examined on the merits.

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Allowable Subject Matter

3. Applicant notes that the Examiner has withdrawn the prior indication of allowable subject matter in claims 12, 15-22, 32, and 33-36.

Rejection Under 35 U.S.C. § 102

5. The Examiner rejects claims 29-32 under 35 U.S.C. § 102(b) as being anticipated by DeLong (6,141,344).

Regarding claim 29, the Examiner asserts that DeLong discloses at least two shared-memory switch fabrics citing the disclosure of I/O ASICs 12 and 14 in Figure 1. Applicant respectfully disagrees. DeLong discloses one and only one switch fabric 22 that interconnects the I/O ASICs 12, 14, 16, and 18. Col. 3, line 66, through col. 4, line 2. One of ordinary skill in the art would understand DeLong to disclose that the I/O ASICs are not switch fabrics because DeLong specifically discusses the use of a switch fabric, such as a crosspoint ASIC, in connection with the disclosure of the I/O ASICs, thereby implying that the I/O ASICs are not crosspoint ASICs or other forms of switch fabrics.

The Examiner further asserts that DeLong discloses storing the packets distributed from the crossbar switch fabric in a shared buffer memory associated with each shared-memory switch fabric citing the step of loading a received data unit in memory as disclosed in col. 5, lines 63-67. Applicant respectfully submits that this does not disclose storing the packets distributed from the crossbar switch fabric. De Long discloses that the received data unit is loaded into memory to determine the destination address. Thus it is clear that DeLong discloses loading the received data unit into memory before distributing the data unit to the crossbar switch fabric 22.

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Regarding claim 30, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

Regarding claim 31, the Examiner asserts that DeLong discloses distributing packets from one of the plurality of ports of the crossbar switch fabrics to more than one of the shared-memory switch fabrics without reference to the final port destination of the packets citing disclosure of loading a received data unit in memory as disclosed in col. 5, lines 63-67. Applicant respectfully disagrees. DeLong discloses one and only one switch fabric 22 and cannot disclose distributing packets from a crossbar switch fabric to a shared-memory switch fabric. Even if the I/O ASICS were considered to be shared-memory switch fabrics, the distribution from the disclosed crossbar switch fabric 22 to an I/O ASIC is done with reference to the final port destination of the packets. Col. 6, lines 3-4.

Regarding claim 32, the Examiner asserts that DeLong discloses that each shared-memory switch fabric is configured to send a packet buffer number indicating where a packet is stored in a shared buffer memory citing the disclosure of col. 5, line 60, through col. 6, line 4. Applicant respectfully disagrees. The cited disclosure discloses a method for determining the specified destination address of a received data unit. This is entirely unlike the claimed element of sending information to an ingress port controller that provides the information about where the packet is stored rather than where the packet is destined. Further, the Examiner fails to indicate what in DeLong discloses an ingress port controller and what discloses that the information includes which shared-memory switch fabric stored the packet.

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Applicant respectfully requests that the Examiner withdraw the rejection of claims 29-32 under 35 U.S.C. § 102(b) as being anticipated by DeLong.

Rejection Under 35 U.S.C. § 103

7. The Examiner rejects claims 1, 2, 4-24, and 33-35 under 35 U.S.C. § 103(a) as being unpatentable over DeLong in view of Ganmukhi et al. (US 5,953,314).

Regarding claim 1, the Examiner asserts that DeLong discloses at least two shared-memory switch fabrics citing the disclosure of I/O ASICs 12 and 14 in Figure 1. Applicant respectfully disagrees. DeLong discloses one and only one switch fabric 22 that interconnects the I/O ASICs 12, 14, 16, and 18. Col. 3, line 66, through col. 4, line 2. One of ordinary skill in the art would understand DeLong to disclose that the I/O ASICs are not switch fabrics because DeLong specifically discusses the use of a switch fabric, such as a crosspoint ASIC, in connection with the disclosure of the I/O ASICs, thereby implying that the I/O ASICs are not crosspoint ASICs or other forms of switch fabrics. Therefore the art cited by the Examiner does not teach or suggest all the elements of the claim.

The Examiner admits that DeLong does not disclose at least two crossbar switch fabrics. The Examiner asserts that Ganmukhi teaches a hybrid network switch that provides a second crossbar switch citing elements 16 and 18 of Figure 1. The Examiner asserts that it would have been obvious to apply the teachings of Ganmukhi to DeLong to reduce susceptibility of to switching failure as taught by the redundant configuration of the two crossbar switch fabrics of Ganmukhi.

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Applicant respectfully points out that Ganmukhi teaches that the I/O cards are interconnected through both switch fabric cards so the system is fully operable regardless of which switch fabric card is in active use, consistent with the redundant architecture for reliability. Col. 2, lines 41-47. The present invention is directed to a scalable architecture and not to a redundant architecture. Specification, page 9, lines 1-11. Applicant has amended claim 1 to add that the plurality of ports for each crossbar switch fabric is unique to that crossbar switch fabric to make the scalable structure of the claimed switch clear. Therefore if the references were combined in the manner suggested by Ganmukhi the resulting combination would be the redundant arrangement disclosed by Ganmukhi and not the claimed scalable arrangement.

Regarding claim 2, the Examiner asserts that the I/O ASICs disclosed by DeLong teaches an NxN shared-memory switch fabric reasoning that the send/receive ports represent N inputs and that the same N ports represent N outputs and therefore the I/O ASIC is an NxN shared-memory switch fabric. Applicant respectfully disagrees. As previously discussed, the I/O ASICs do not teach or suggest shared-memory switch fabrics. Even if the I/O ASICs are considered to suggest shared-memory switch fabrics, they would be identified as 1xN devices for N send/receive ports and the 1 connection to the switch fabric. It is inherent in an NxM switch fabric that any of the N inputs can be connected to any of the M outputs. Nothing in DeLong teaches or suggests that it is possible to connect any of the N send/receive ports together. Therefore DeLong does not teach or suggest an NxN shared-memory switch fabric.

Regarding claims 4-10, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional elements recited.

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Regarding claim 11, the Examiner asserts that the control processor 12/14 disclosed by Ganmukhi teaches a port controller. Applicant has amended the claim to add elements that make clear that the claimed port controller is coupled to the plurality of ports of the crossbar switch fabric and to the network connection. This clearly distinguishes the claimed port controller from the control processor disclosed by Ganmukhi which is not coupled to either the ports of the crossbar switch fabric or to the network connection. Thus Ganmukhi does not disclose the port controller as now claimed. Further the Examiner asserts that it would have been obvious to combine the teachings of Ganmukhi to DeLong in order to reduce the susceptibility to switching failure. However it is the redundancy of the design taught by Ganmukhi that would reduce the susceptibility to switching failure. Applicant fails to see why it would be obvious to combine the control processor of Ganmukhi with the device disclosed by DeLong to reduce the susceptibility to switching failure. Even if the teachings of Ganmukhi are combined with the device taught by DeLong, this would not result in a device as now claimed because the control processor would not be coupled to the crossbar switch fabric or to the network connection as now claimed.

Regarding claim 12, the Examiner asserts that the timing control module 20/22 disclosed by Ganmukhi teaches a notify ring. Applicant has amended the claim to add elements that make clear that the claimed notify ring is configured to transfer forwarding information from a first of the plurality of port controllers to a second of the plurality of port controllers. This clearly distinguishes the claimed notify ring from the timing control module disclosed by Ganmukhi which is not configured to transfer forwarding information from the first control processor to the second control processor because only one of the control processors is active with the other being in standby. Col. 3, lines 12-28. Thus Ganmukhi does not disclose the notify ring as now claimed. Further the Examiner asserts that it would have been obvious to combine the teachings

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of Ganmukhi to DeLong in order to reduce the susceptibility to switching failure. However it is the redundancy of the design taught by Ganmukhi that would reduce the susceptibility to switching failure. Applicant fails to see why it would be obvious to combine the timing control module of Ganmukhi with the device disclosed by DeLong to reduce the susceptibility to switching failure. Even if the teachings of Ganmukhi are combined with the device taught by DeLong, this would not result in a device as now claimed because the timing control module would not transfer forwarding information from a first port controller to a second port controller as now claimed.

Regarding claim 13, the Examiner asserts that De Long teaches the crossbar switch 22 is configured to distribute packets to the I/O ASICs 12/14 which the Examiner considers to read on the shared-memory switch fabrics. The Examiner fails to address the element of the claim that the distribution is without reference to the final port destination of the packets. DeLong teaches away from this limitation in that data units are examined after receipt for an address indicator field that pertains to the destination address so that the data unit can be forwarded toward the destination device. Col. 4, lines 17-39. Thus DeLong teaches that the distribution is with particular reference to the final port destination of the packets which is quite distinct from the claimed limitation of distribution without reference to the final port destination of the packets.

Regarding claim 14, the Examiner asserts that DeLong teaches that the I/O ASICs 12/14 which the Examiner considers to read on the shared-memory switch fabrics are configured to store packets in a shared buffer memory. The Examiner fails to address the element of the claim that the shared-memory switch fabric is configured to store and retrieve the distributed packets from the crossbar switch fabrics. Applicant is unable to find anything in DeLong that teaches or

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suggests that the I/O ASICs are configured to retrieve the data units from the crossbar switch fabrics.

Regarding claim 15, the Examiner asserts that DeLong teaches each shared-memory switch fabric is configured to send a packet buffer number indicating where a packet is stored in a shared buffer memory. The Examiner considers that the destination address reads on the claimed packet buffer number. This overlooks that the destination address does not indicate where a packet is stored in a shared buffer memory, a temporary location within the switch. The destination address indicates what the destination device is. Col. 4, lines 27-39.

Regarding claims 16, 17, 33, and 34, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional elements recited.

Regarding claims 18, 21, and 35, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional elements recited.

Regarding claim 22, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

Regarding claims 23 and 24, applicant relies on the patentability of the claims from which these claims depend to traverse the rejection without prejudice to any further basis for patentability of these claims based on the additional elements recited.

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Applicants respectfully request that the Examiner withdraw the rejection of claims 1, 2, 4-24, and 33-35 under 35 U.S.C. § 103(a) as being unpatentable over DeLong in view of Ganmukhi.

8. The Examiner rejects claim 36 under 35 U.S.C. § 103(a) as being unpatentable over DeLong.

Regarding claim 36, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

Applicants respectfully request that the Examiner withdraw the rejection of claim 36 under 35 U.S.C. § 103(a) as being unpatentable over DeLong.

Conclusion

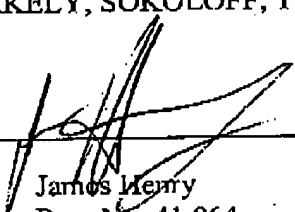
Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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By


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